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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,872	11/08/2001	John Lin	BP1907	5330

51472 7590 06/01/2010

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EXAMINER	
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ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
06/01/2010	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN LIN and VIVIAN CHOU

Appeal 2009-004527
Application 10/008,872
Technology Center 2100

Decided: May 27, 2010

Before JAMES D. THOMAS, JOSEPH L. DIXON,
and DEBRA K. STEPHENS, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1, 3, 5 through 7, 11 through 17, and 20 through 22. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse both rejections under 35 U.S.C. § 103 and institute a new ground of rejection within the provisions of 37 C.F.R. § 41.50(b).

INVENTION

A baseband controller system includes a master to a multi-slave asynchronous transmit FIFO structure that enables the traffic to all slaves to be independent of each other in a manner that reduces the shortcomings of traditional FIFO structures. The inventive FIFO structure includes a plurality of pointer blocks wherein each of the FIFO pointer blocks comprises a plurality of one-byte pointers that point to command blocks. The command blocks, in turn, define an address that points to a starting address of a data block. (Spec. 33, ll. 2-10, Figs. 3, 6, and 7.)

REPRESENTATIVE CLAIM

1. A wireless transceiver device, comprising:

modulation circuitry for modulating and demodulating signals that are transmitted over airwaves;

frequency conversion circuitry for up converting and down converting between radio frequency signals and baseband frequency signals;

digital-to-analog conversion circuitry for converting from analog to digital and from digital to analog;

a radio controller;

baseband processing circuitry including a first in, first out (FIFO) memory structure for storing addresses for accessing data blocks; and

a plurality of command blocks formed within a memory structure, the command blocks include addresses of data blocks stored within random access memory and a memory portion for storing an indicator for indicating whether a command block of the plurality of command blocks is in use.

PRIOR ART AND EXAMINER'S REJECTIONS

The Examiner relies on the following references as evidence of unpatentability:

Chisholm	US 5,968,143	Oct. 19, 1999
Fesas	US 2002/0009075 A1	Jan. 24, 2002 (filed Jul. 24, 1997)
Micalizzi	US 6,434,630 B1	Aug. 13, 2002 (filed Mar. 31, 1999)
Auckland	US 2002/0183013 A1	Dec. 5, 2002 (filed May 25, 2001)

Claims 1, 3, 5 through 7, 11 through 17, 20, and 22 stand rejected under 35 U.S.C. § 103 as being obvious over Auckland in view of Chisholm, further in view of Micalizzi. To this combination of references, the Examiner adds Fesas as to claim 21.

ANALYSIS

For the reasons set forth subsequently in this opinion, with respect to all claims on appeal, claims 1, 3, 5 through 7, 11, 20, and 22, the existing

prior art rejections must be reversed *pro forma* because they are necessarily based on speculative assumptions and inferences as to the meaning of the claims. *See In re Steele*, 305 F.2d 859, 862-863 (CCPA 1962). It should be understood, however, that our decision in this regard is based solely on the indefiniteness of the claimed subject matter and does not reflect the adequacy or the inadequacy of the prior art evidence applied in support of the rejection before us. Once definite claims are presented, the Examiner is free to apply the same, different, or additional prior art if the Examiner so chooses.

New Rejection within 37 C.F.R. § 41.50(b)

Claims 1, 3, 5 through 7, 11 through 17, 20, and 22 are rejected under the second paragraph 35 U.S.C. § 112 as being indefinite.

All claims on appeal variously recite terms such as memory structure, FIFO memory structure, memory portions, and the like. The use of these terms is ambiguous since it cannot be reasonably determined if these claims are directed to hardware elements or merely to descriptive elements or both. These terms and such terms as command blocks, data blocks, memory portions, indicators, memory pointers, and the like appear to be directed merely to ambiguous data structures based upon the disclosed invention. The manner in which the subject matter of each independent claims 1, 7, and 17 is written appears to predicate patentability upon these broadly defined, ambiguous, labels of data that are not recited to have a functional

relationship with any recited substrate and do not appear to affect the manner in which processes or functions are performed as recited.

The labels or content of this nonfunctional descriptive material is not entitled to weight in the patentability analysis. Such nonfunctional descriptive material does not further limit the claimed invention either functionally or structurally. *In re Ngai*, 367 F.3d 1336, 1339 (Fed. Cir. 2004). *See also Ex parte Nehls*, 88 USPQ2d 1883, 1887-89 (Bd. Pat. App. & Int. 2008) (precedential) (discussing cases pertaining to non-functional descriptive material); *Ex parte Mathias*, No. 2005-1851 (Bd. Pat. App. & Int. Aug. 19, 2005), *aff'd. In re Mathias*, No. 2006-1103, WL 2433879 (Fed. Cir. Aug. 17, 2006) (Rule 36, unpublished); *Ex parte Curry*, No. 2005-0509 (Bd. Pat. App. & Int. June 30, 2005), *aff'd In re Curry*, No. 2006-1003 (Fed. Cir. Jun. 12, 2006) (Rule 36, unpublished) (both cases treating data as nonfunctional descriptive material).

As to independent claim 1 on appeal, the variously recited circuit elements are not stated to cooperate with each other, let alone with the label-described recitations at the and of this claim. Essentially, this claim recites hardware elements only in a disconnected, laundry list form. As such, this claim clearly is indefinite. As to independent claim 7, the body of this claim does not recite any transmission of data as set forth in the preamble of this claim. The claimed defined memory location is not defined nor has it been previously recited. Independent claim 17 recites in its preamble a baseband processing system to which the body of this claim does not refer.

CONCLUSION AND DECISION

We have *pro forma* reversed the two outstanding rejections under 35 U.S.C. § 103 that encompass all claims on appeal, claims 1, 3, 5 through 7, 11 through 17, and 20 through 22. We have instituted our own rejection of all these claims on appeal under 35 U.S.C. § 112, second paragraph.

A new ground of rejection is pursuant to 37 C.F.R. § 41.50(b). 37 C.F.R. § 41.50(b) provides that, "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new grounds of rejection to avoid termination of proceedings (37 C.F.R. § 1.197 (b)) as to the rejected claims:

> (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner ….
>
> (2) *Request rehearing*. Request that the proceeding be reheard under 37 C.F.R. § 41.52 by the Board upon the same record ….

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(iv).

REVERSED
37 C.F.R. § 41.50(b)

rwk

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